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18EC72

Seventh Semester B.E. Degree Examination, Feb./Mar. 2022
VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. With necessary circuit diagram, explain the operation of tristate inverter. Also realize a 2 : 1 multiplexer using tristate inverter. **(08 Marks)**

b. Implement a D flipflop using transmission gates and explain its operation with necessary tining diagram. **(08 Marks)**

c. Realize CMOS compound gate for the function $Y = \overline{A(B+C)+DE}$. **(04 Marks)**

OR

2 a. Explain the operation of MOSFET with necessary diagrams. Also derive the equation for drain current in linear and saturation region of operation. **(10 Marks)**

b. Draw the circuit of CMOS inverter and explain its DC transfer characteristics. **(06 Marks)**

c. Explain the following non-ideal effects channel length modulation, mobility degradation. **(04 Marks)**

Module-2

3 a. Explain CMOS n-well fabrication process with necessary diagrams. **(12 Marks)**

b. What is scaling. Compute drain current, power, current density and power density for constant field and constant voltage scaling. **(08 Marks)**

OR

4 a. Draw the layout of $Y = \overline{(A+B+C)D}$ and estimate the area. **(08 Marks)**

b. Mention different types of MOSFET capacitances and explain with necessary diagrams and equations. **(06 Marks)**

c. With neat diagram, explain lambda based design rules for wires and contacts. **(06 Marks)**

Module-3

5 a. Develop the RC delay model to compute the delay of the logic circuit and calculate the delay of unit sized inverter driving another unit inverter. **(08 Marks)**

b. Explain Cascode Voltage Switch Logic (CVSL). Also realize two input AND/NAND using CVSL. **(06 Marks)**

c. Explain linear delay model. Compare the logical efforts of the following gates with the help of schematic diagrams :
i) 2-input NAND gate ii) 3-input NOR gate. **(06Marks)**

OR

6 a. Explain : i) pseudo nMOS ii) ganged CMOS with necessary circuit examples. **(06 Marks)**

b. Estimate t_{pdf} and t_{pdr} of a 3-input NAND gate if the output is loaded with h identical gates. Use Elmore delay model. **(08 Marks)**

c. Explain skewed gates with an example. **(06 Marks)**

Module-4

7 a. With necessary circuit diagrams, explain resettable latches with
i) synchronous reset
ii) asynchronous reset. **(08 Marks)**

b. Compute the output voltage V_{out} in the following pass transistor circuits. Assume $V_t = 0.7$. (Ref. Fig.Q7(b)).

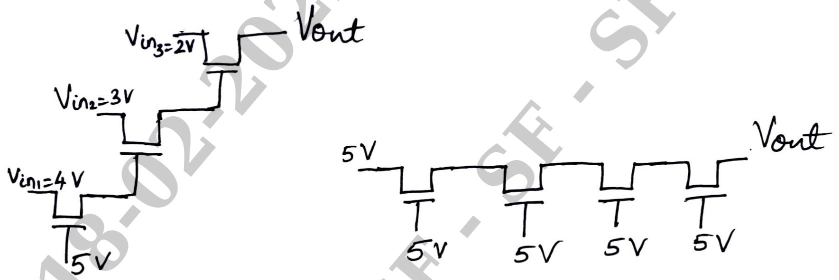

Fig.Q7(b) **(06 Marks)**

c. With necessary diagram, explain a D flipflop with two-phase non-overlapping clocks. **(06 Marks)**

OR

8 a. With necessary circuit diagram explain 3-bit dynamic shift register with depletion load. **(08 Marks)**

b. Realize $F = \overline{A_1A_2A_3 + B_1B_2}$ using dynamic CMOS logic. Also explain the cascading problem in dynamic logic with necessary example. **(08 Marks)**

c. Explain the general structure of ratioless synchronous dynamic logic with relevant diagram. **(04 Marks)**

Module-5

9 a. With necessary circuit diagram, explain the operation of three transistor DRAM cell. **(08 Marks)**

b. Explain full CMOS SRAM cell with necessary circuit topology. **(08 Marks)**

c. Explain the terms :
i) Observability
ii) Controllability
iii) Fault coverage. **(04 Marks)**

OR

10 a. What is a fault model? Explain stuck-at model with examples. **(07 Marks)**

b. Mention the approaches used in design for testability. Explain scan based testing using necessary diagrams. **(07 Marks)**

c. Draw the circuit of 3-bit BIST register and explain. **(06 Marks)**

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